RISC-V®

PAST, PRESENT, FUTURE

Krste Asanovic
Prof. EECS, UC Berkeley;
Chairman of the Board,
RISC-V Foundation;
Co-Founder and Chief Architect,
SiFive Inc.

@risc_v

Why Instruction Set Architecture matters

- **Why can't Intel sell mobile chips?**
  - 99%+ of mobile phones/tablets based on ARM v7/v8 ISA
- **Why can't ARM partners sell servers?**
  - 99%+ of laptops/desktops/servers based on AMD64 ISA (over 95%+ built by Intel)
- **How can IBM still sell mainframes?**
  - IBM 360, oldest surviving ISA (50+ years)

ISA is most important interface in computer system

where software meets hardware

Open Interfaces Work for Software!

Field	*Open Standard*	*Free, Open Impl.*	*Proprietary Impl.*
Networking	Ethernet, TCP/IP	Many	Many
OS	Posix	Linux, FreeBSD	M/S Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, M/S DB2
Graphics	OpenGL	Mesa3D	M/S DirectX
ISA	??????	----------	x86, ARM, IBM360

- Why not successful free & open standards and free & open implementations, like other fields?
- Dominant proprietary ISAs are not great designs

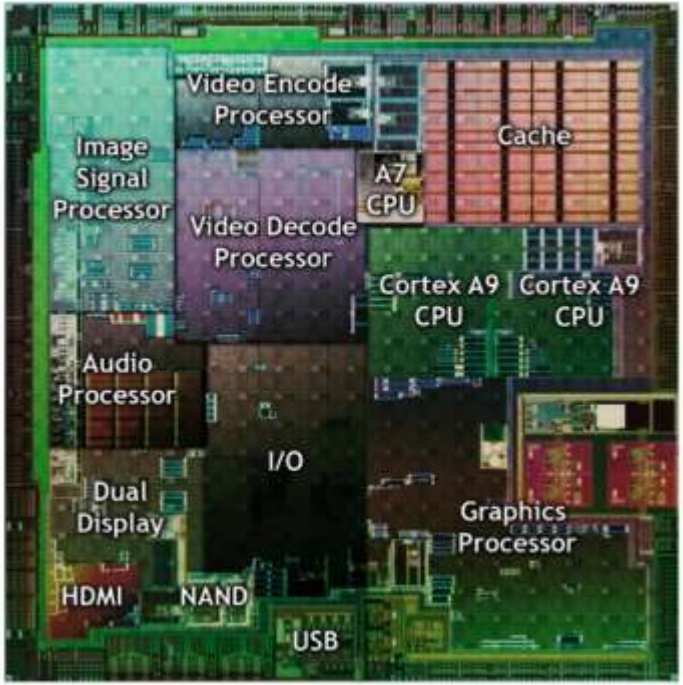
Companies and their ISAs Come and Go

Proprietary ISA fortunes tied to business fortunes and whims

- Digital Equipment Corporation
  - **PDP-11**, **VAX**, **Alpha**
- Intel
  - **i960**, **i860**, **Itanium**
- **MIPS**
  - Sold to Imagination, then bought by Wave AI startup, now opening R6?
- **SPARC**
  - Was opened by Sun, acquired by Oracle, now closed down
- **ARM**
  - Sold to Softbank at >40% premium
  - Now 25% sold off to Abu Dhabi investment fund

Today, many ISAs on one SoC

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- *> dozen ISAs on some SoCs – each with unique software stack*



NVIDIA Tegra SoC

Why?

- Apps processor ISA too big, inflexible for accelerators
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores

Do we need all these different ISAs?

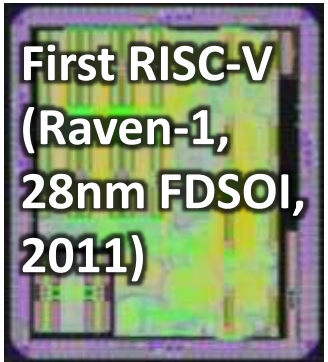
Must they be proprietary?

Must they keep disappearing?

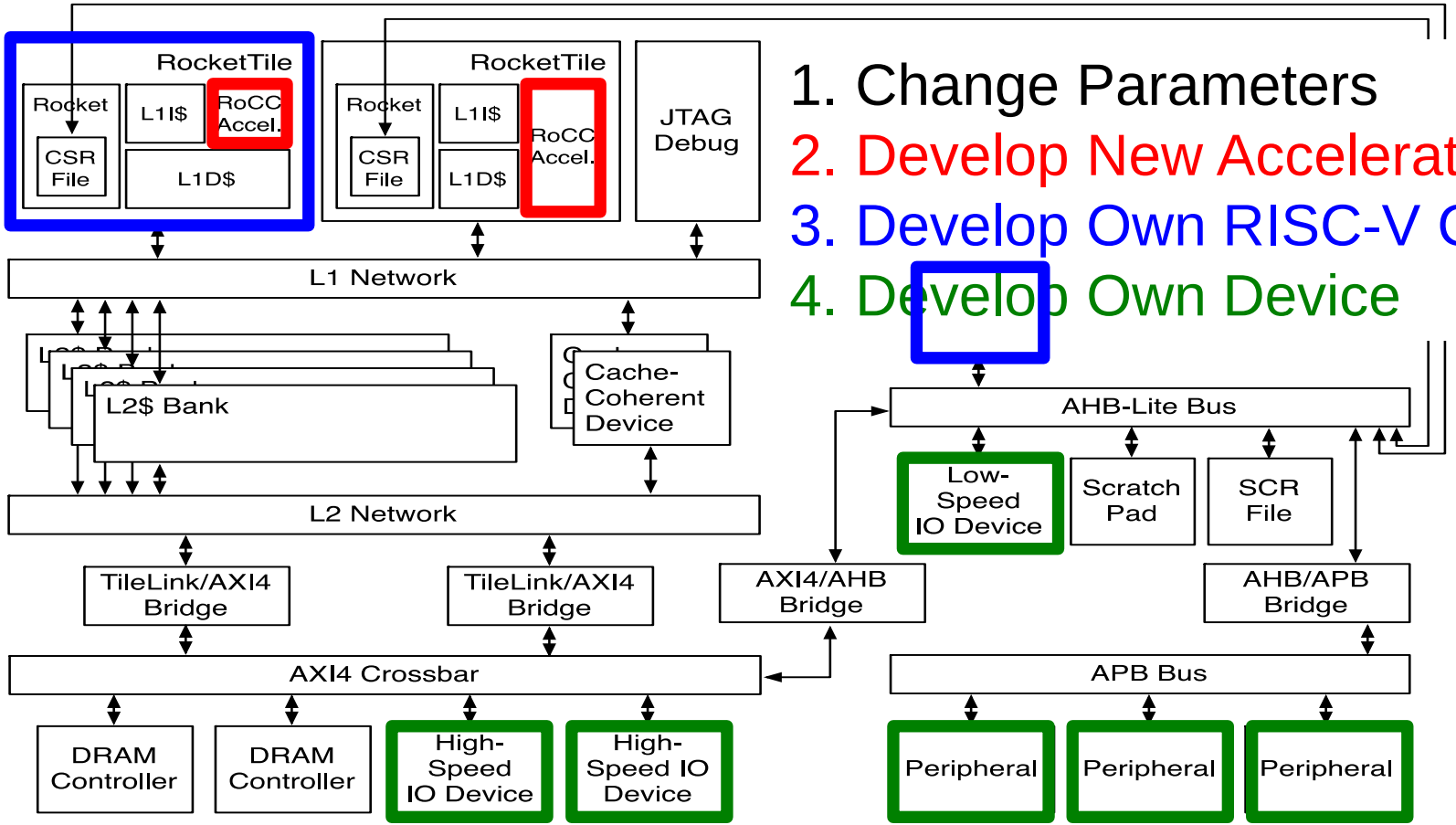
What if there was one stable free and open ISA everyone could use for everything?

RISC-V Background

- In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects
- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, no 64-bit in 2010, IP issues
- So we started "3-month project" during summer 2010 to develop clean-slate ISA
  - Principal designers: Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanovic
- Four years later, May 2014, released frozen base user spec
  - many tapeouts and several research publications along the way
- Name RISC-V (pronounced "risk-five") represents fifth major Berkeley RISC ISA

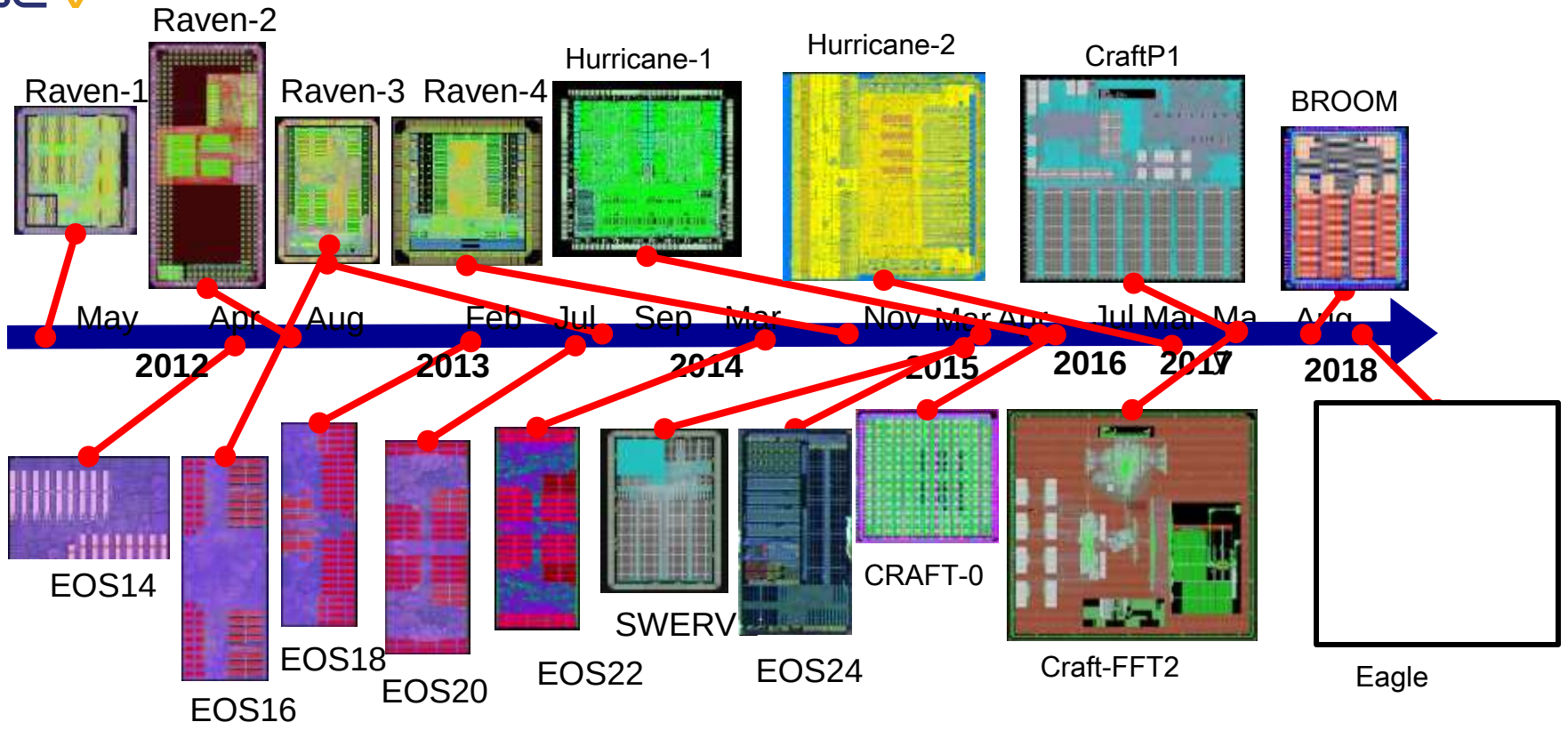


Open-Source RISC-V Rocket Chip Generator



1. Change Parameters
2. Develop New Accelerators
3. Develop Own RISC-V Core
4. Develop Own Device

RISC-V SoCs Designed in Berkeley



In IBM 45nm, ST 28nm FDOI, TSMC 28nm and 16nm FF, GF 14nm

Benefits of RISC-V

Dave Ditzel, Esperanto

RISC-V wasn't even on the shopping list of alternatives, but the more Esperanto's engineers looked at it, the more they realized it was more than a toy or just a teaching tool. "We assumed that RISC-V would probably lose 30% to 40% in compiler efficiency [versus Arm or MIPS or SPARC] because it's so simple," says Ditzel. "But our compiler guys benchmarked it, and darned if it wasn't within 1%."

[Article by Jim Turley, EE Journal, December 13, 2017]

Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices

Why is RISC-V so popular?

- Engineers sometimes "*don't see forest for the trees*"
- The movement is ***not*** happening because some benchmark ran 10% faster, or some implementation was 30% lower power
- The movement ***is*** happening because ***new business model*** changes everything
  - Pick ISA first, then pick vendor or build own core
  - Add your own extension without getting permission
- Implementation features/PPA will follow
  - Whatever is broken/missing in RISC-V will get fixed

The RISC-V Foundation—Today

A non-profit corporation governed by an elected board of directors

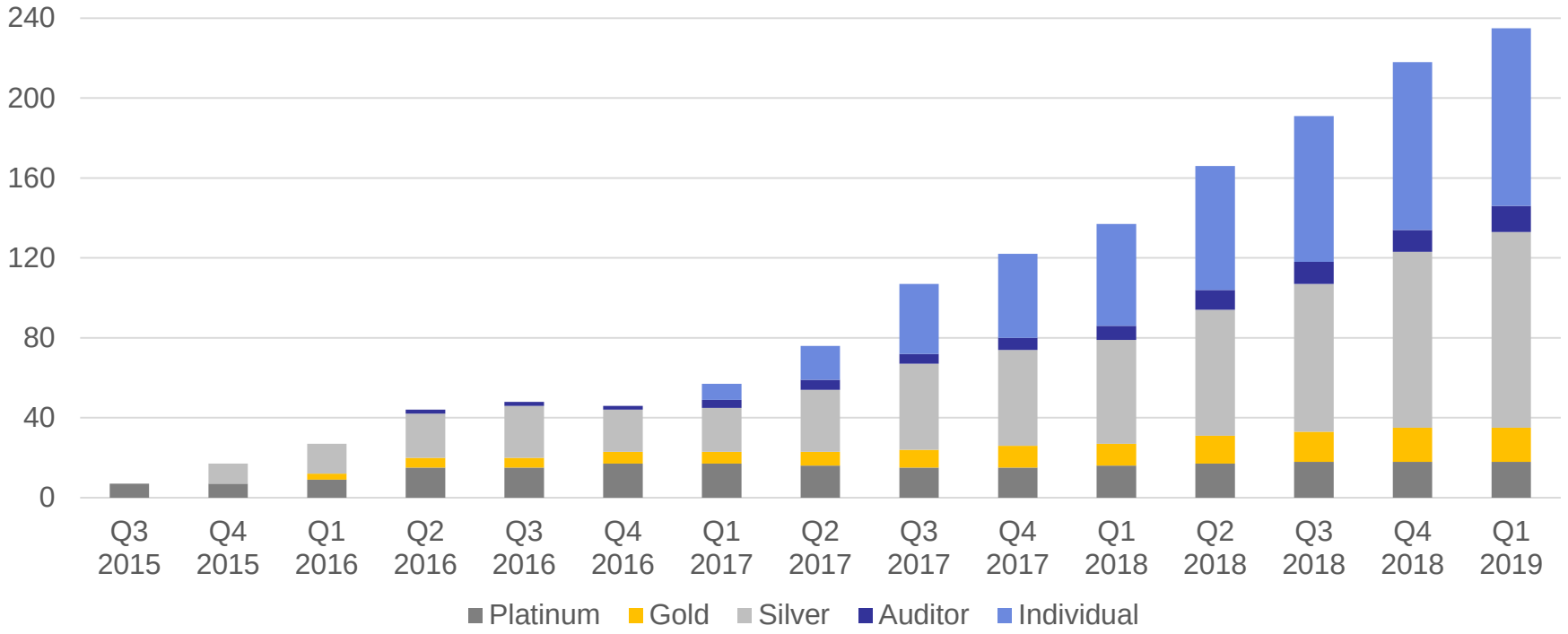
- Develop, ratify, and maintain the RISC-V ISA and related specifications
- Grow Membership
- Create awareness

RISC-V Foundation Board of Directors

- Krste Asanović, Chairman
  - Professor in the EECS Department at **UC Berkeley**, Chief Architect, **SiFive**
- David Patterson, Vice-Chairman
  - **Google** Architect, Retired Professor Computer Science UC Berkeley
- Zvonimir Bandić
  - Senior Director of Next Generation Platform Technologies at **Western Digital** Corporation
- Charlie Hauck
  - CEO of **Bluespec** Inc.
- Rob Oshana
  - Director Global SW Development at **NXP**
- Frans Sijstermans
  - Vice President Engineering at **NVIDIA**
- Ted Speers
  - Technical Fellow, Head of Product Architecture for **Microsemi** SoC Group

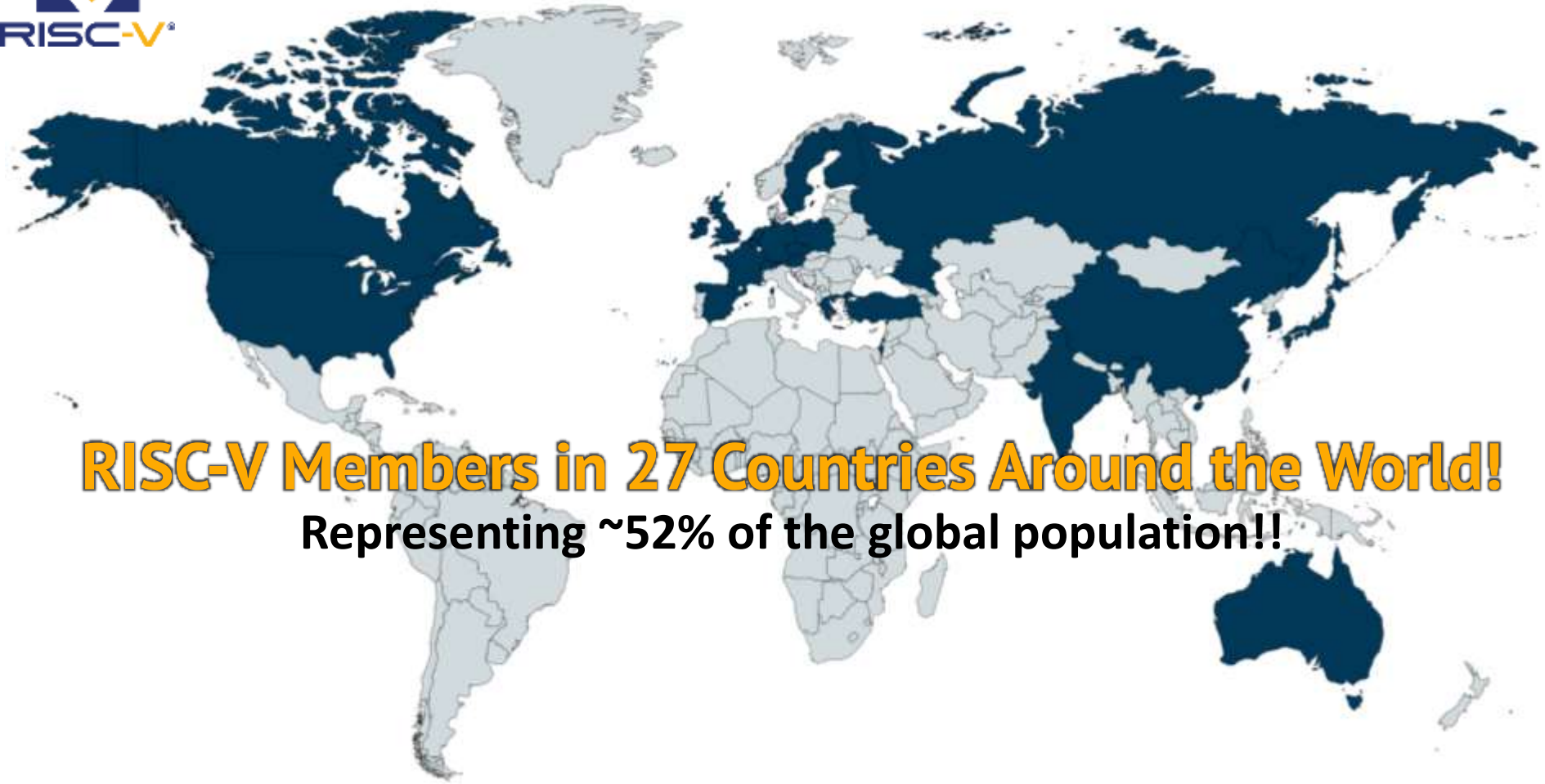
RISC-V Foundation Growth

September 2015 – February 2019




RISC-V
SEMICONDUCTOR IP
IP AND DESIGN SERVICES
FOUNDRY SERVICES
ANDES TECHNOLOGY
cortus
INTRINSIC ID
CEVA
Roo Logic
inside secure
Esperanto TECHNOLOGIES
Rambus
DOVER MICROSYSTEMS
ultraSoC
SECURE RF
bluespec
codasip
DOLPHIN INTEGRATION
SiFive
C-SKY
XtremeEDA
Rumble Development
UO TECH IP
VeriSilicon
Minima
dxcorr
Syntacore
Intrinsix
VectorBlox
GLOBAL FOUNDRIES
CONSULTING/RESEARCH
NUS
PRINCETON UNIVERSITY
ETH zürich
Berkeley Architecture Research
FORTH
MIT CSAIL
DRAPER
galois
DATA 61
Technolution
CMC
lowRISC
SHC
DEVELOPMENT TOOLS
SW AND CLOUD
SEGGER
IAR SYSTEMS
antmicro
ASHLING
LAUTERBACH
imperas
MINRES
Symbiotic EDA
Mentor
cadence
runtime.io
Google
HEX-Five Security
Alibaba.com
HORTONWORKS
expresslogic
MACHINE LEARNING/AI
COMMERCIAL CHIP VENDORS
FPGA
NETWORKING
BROAD MARKET
APPLICATION PROCESSORS, GRAPHICS
Micron
LATTICE
pango
QuickLogic
Microsemi
SEAGATE
SK hynix
Western Digital
MEDIATEK
QUALCOMM
SANECHIPS
NVIDIA
SAMSUNG
Esperanto TECHNOLOGIES
NXP
IDT
MARVELL
GREENWAVES
HUAWEI
Mellanox
BAE SYSTEMS
SIEMENS
IBM
NORTHROP GRUMMAN

RISC-V Global Growth



RISC-V Members in 27 Countries Around the World!

Representing ~52% of the global population!!

Meetups (1,500+ Members)

Grass-Roots Effort

Bay Area RISC-V Group
https://www.meetup.com/Bay-Area-RISC-V-Meetup/

Rocky Mountain Area RISC-V Group
https://www.meetup.com/Rocky-Mountain-Area-RISC-V-Group/

Austin Area RISC-V Group
https://www.meetup.com/Austin-Area-RISC-V-Group/

Israel RISC-V Meetups
https://www.meetup.com/Israel-RISC-V-meetups/

Cambridge RISC-V Meetup Group
https://www.meetup.com/Cambridge-RISC-V-Meetup-Group/

Bristol RISC-V Meetup Group
https://www.meetup.com/Bristol-RISC-V-Meetup-Group/

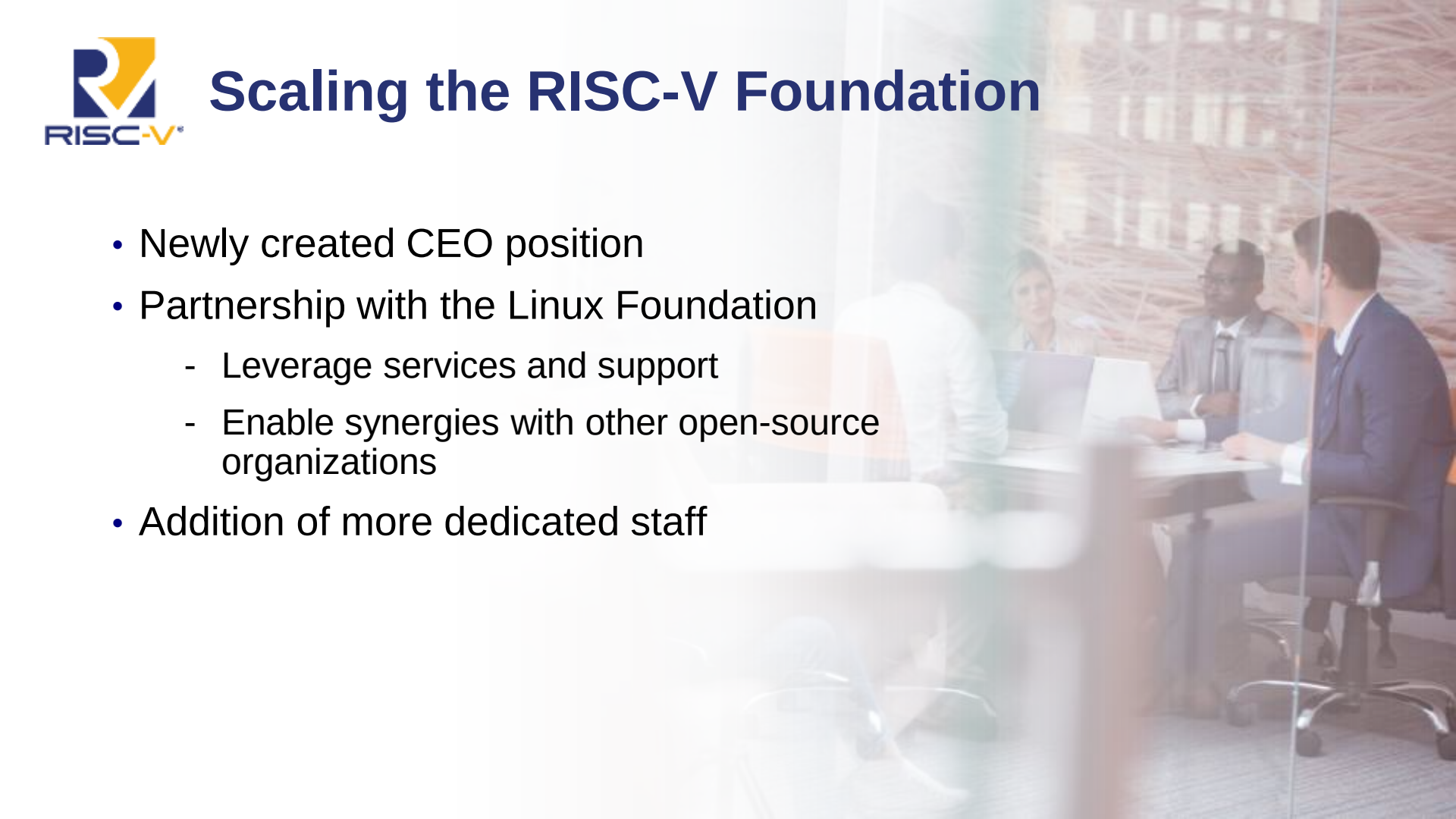
Pune RISC-V Group
https://www.meetup.com/Pune-RISC-V-Group/

Vienna RISC-V Meetup
https://www.meetup.com/Vienna-RISC-V-Meetup/

Shanghai RISC-V Meetup
https://www.meetup.com/shanghai-riscv/

Scaling the RISC-V Foundation

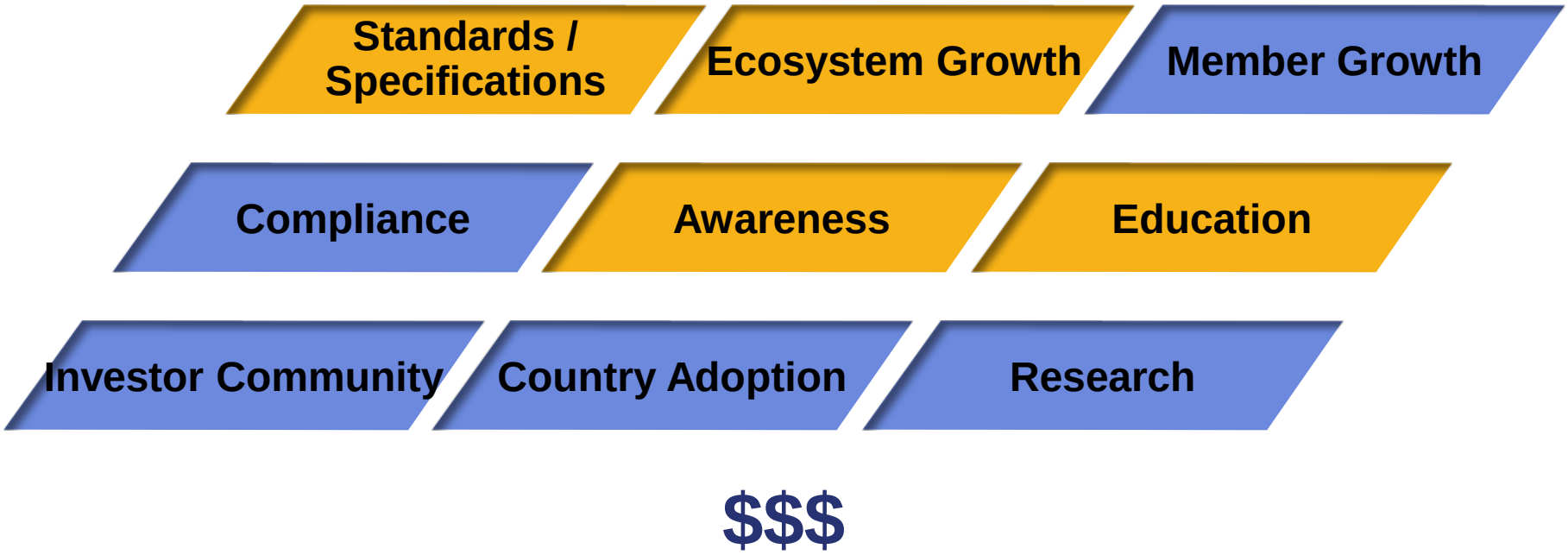
- Newly created CEO position
- Partnership with the Linux Foundation
  - Leverage services and support
  - Enable synergies with other open-source organizations
- Addition of more dedicated staff



Calista Redmond, CEO

Previously, Vice-President of IBM Z Ecosystem division; President of OpenPOWER Foundation.

Foundation Areas of Focus in Future



Raising Awareness

1 Major Annual Summit (San Jose) + 2 Workshops (Zurich & Taiwan)

- Expecting to grow the number and size

15 One-Day events

- US (Milpitas, Irvine, Austin, Boston)
- China (Beijing, Shanghai, Hanzhou, Shenzhen, Chengdu)
- Europe (UK, Munich, Berlin, Paris, Tel Aviv, Estonia)

Sponsored webinars

Continue working with members on grass root initiatives

- Meetups
- ***Member-held events***

Education

- Develop Education Resources At All Levels
- Drive Adoption By Universities
- Develop Corporate Education Partnership Programs to Reach Students Globally

- Drive the Development of Low Cost Boards
- Develop a Training Certification Program
- Develop Online Training Modules

Foundation's Value for Members

- Ability to drive standards and set direction on future specifications
- Use of the RISC-V trademarks and logos
- Several RISC-V Foundation Groups for support (technical, marketing, educational, etc)
- Strong ecosystem for support
- Marketability to a large client base
- Exposure to global markets

RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, Imperas, …

RISC-V Foundation

ISA specification | Golden Model | Compliance

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Swerv, Hummingbird, …

Commercial core providers:
Andes, Bluespec, Cloudbear, Codasip, Cortus, C-Sky, Nuclei, SiFive, Syntacore, …

Inhouse cores:
Nvidia, +others

Foundation ISA Standards Development

- Unprivileged base and initial extensions now formally ratified
  - RV32IMFDC, RV64IMFDC
  - ”A” extension has one minor issue to resolve (LR/SC progress)
  - User ISA stable since 2014 release
- Privileged spec formally ratified
- Multiple Formal models available, in public review right now
- Vector specification 0.7 released as stable draft in January 2019
  - Largest single extension to date
  - Target of advanced implementation work
- Other new ISA modules in advanced development:
  - Fast interrupts, DSP, Bit manipulation, Hypervisor, …
- Member-driven ISA roadmap

Foundation Working Groups (partial list)

Bit Manipulation

Compliance

Debug

Memory Model

Privileged Spec

Vector

Security

Base ISA / Opcode

The RISC-V Big Tent Philosophy

- Enable all types of RISC-V implementation
  - 32-bit microcontrollers with 1KiB SRAM
  - 64-bit Unix servers with virtualization
  - 128-bit 100,000-core supercomputers with PiBs DRAM
  - Fully open platforms, only open-source software
  - Fully locked-down platforms, completely trusted
  - Platforms with pay-as-you-go hardware and software
  - Platforms with extensive non-conforming extensions
  - QEMU RISC-V containers running on x86 servers
- Minimize wasted work through maximum reuse
  - Factor out platform-level requirements from reusable ISA and SW modules
- Use standard platform profiles to reduce ecosystem effort
  - Platform profiles tightly constrain choices among all options

Fragmentation versus Diversity

Fragmentation:
Same thing done different ways

Diversity:
Solving different problems

RISC-V and Security

Security is one of biggest challenges in contemporary computer architecture, so which to trust?

- Simple free ISA with open implementations and publicly scrutinized security systems
- Baroque proprietary ISAs with complex unauditable implementations of NDA-only security systems

RISC-V already the center of security architecture research

- Small set of hardware primitives support everything from embedded security to remote cloud enclaves

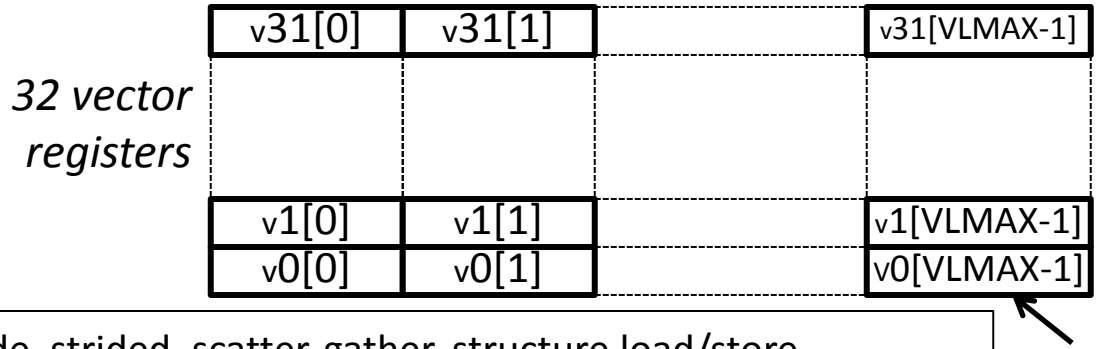
RISC-V Vector Extension Overview

vl

Vector length CSR sets number of elements active in each instruction

vtype

Vtype sets width of element in each vector register (e.g., 32-bit, 16-bit)



- Unit-stride, strided, scatter-gather, structure load/store instructions
- Rich set of integer, fixed-point, and floating-point instructions
- Vector-vector, vector-scalar, and vector-immediate instructions
- Multiple vector registers can be combined to form longer vectors to reduce instruction bandwidth or support mixed-precision operations (e.g., 16b*16b->32b multiply-accumulate)
- Designed for extension with custom datatypes and widths

Maximum vector length (VLMAX) depends on implementation, number of vector registers used, and type of each element.

Industry Adoption Status

- Large companies adopting RISC-V for deeply embedded controllers in their SoCs (“minion cores”)
  - NVIDIA publicly announced all future GPUs will use RISC-V
  - Western Digital publicly announced transition of all billion cores/year to RISC-V
  - Replaces home-grown and commercial cores
  - Others waiting in the wings

CTOs across entire worldwide value chain of IC suppliers, system providers, service providers, are evaluating RISC-V strategies

Replacing 2nd-tier ISAs

- Smaller proprietary-ISA soft-core IP companies switching to RISC-V standard to access larger market:
  - Andes
  - Codasip
  - Cortus
  - C-Sky
  - others to announce

If you're a softcore IP provider,
you should have a RISC-V product in development

Startups

- Many startups choosing RISC-V for new products
- Esperanto announced 4,096-core 7nm RISC-V chip, with high-end OoO cores
- Fadu SSD controller announcement
- Kendryte AI microcontroller, $3 chip with two RISC-V cores from open-source Rocket codebase
- Most are stealthy so will not be visible for a while

We haven't had to tell startups about RISC-V; they find out pretty quickly when shopping for processor IP

Commercial Ecosystem Providers

- Mainstream commercial ecosystem support rapidly appearing
  - Lauterbach, Micrium, Segger, IAR, Express Logic, Imperas, UltraSOC, …

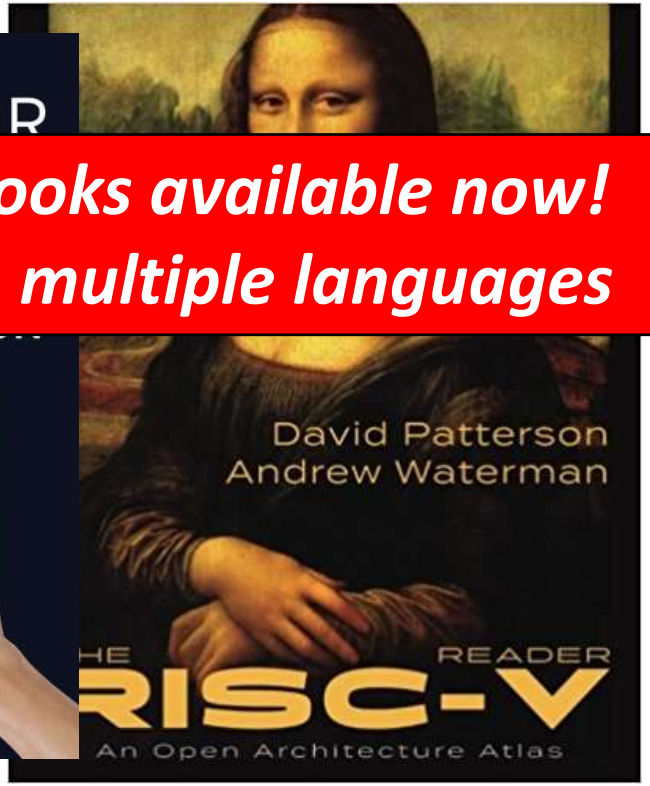
Demand is driving supply in commercial ecosystem

Government Adoption

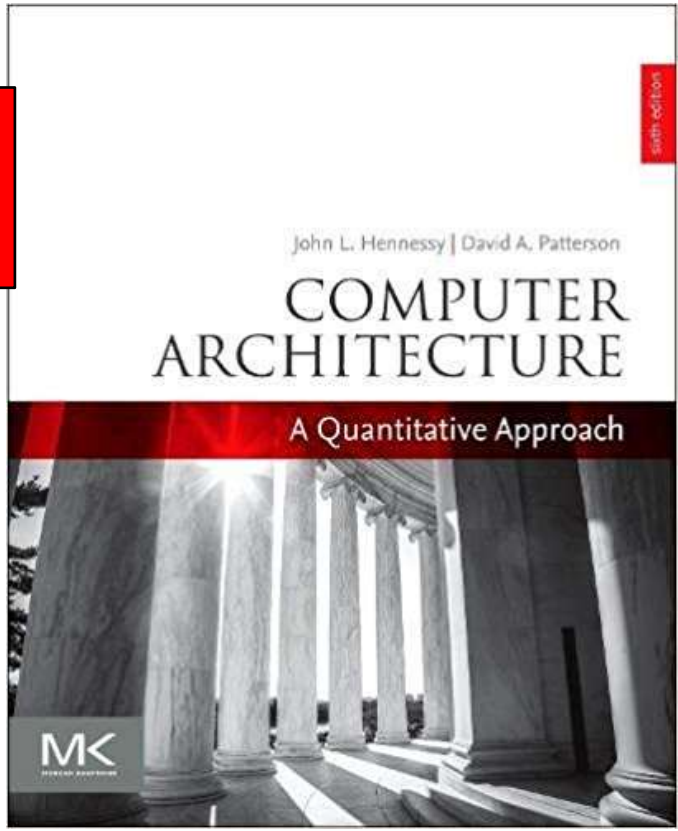
- India has adopted RISC-V as national ISA
- US DARPA mandated RISC-V in recent security call for proposals
- Israel Innovation Authority creating GenPro incubator around RISC-V
- Shanghai Municipal Govt supporting RISC-V companies
- Other governments at various stages of investigation

If your country wishes to control security of its own information infrastructure, and promote its indigenous semiconductor industry, support RISC-V

RISC-V in Education

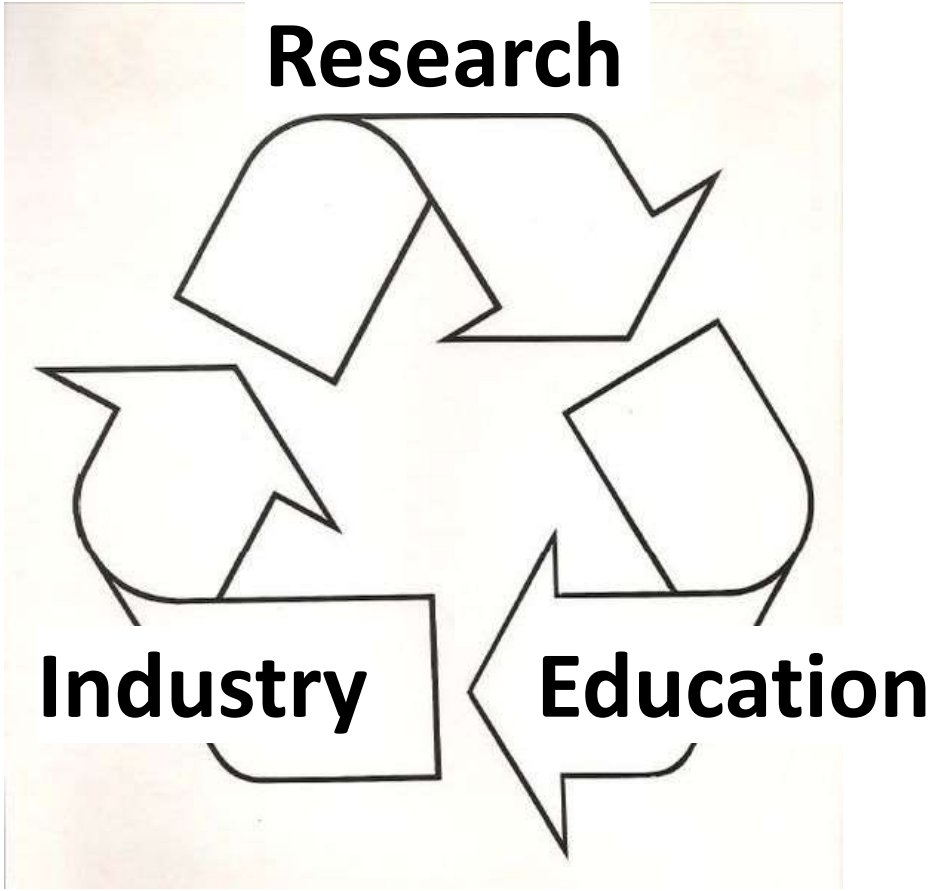


Books available now!
In multiple languages



RISC-V spreading quickly throughout curricula of top schools

RISC-V: Completing the Innovation Cycle



Open ecosystem is key to keeping the virtuous cycle going