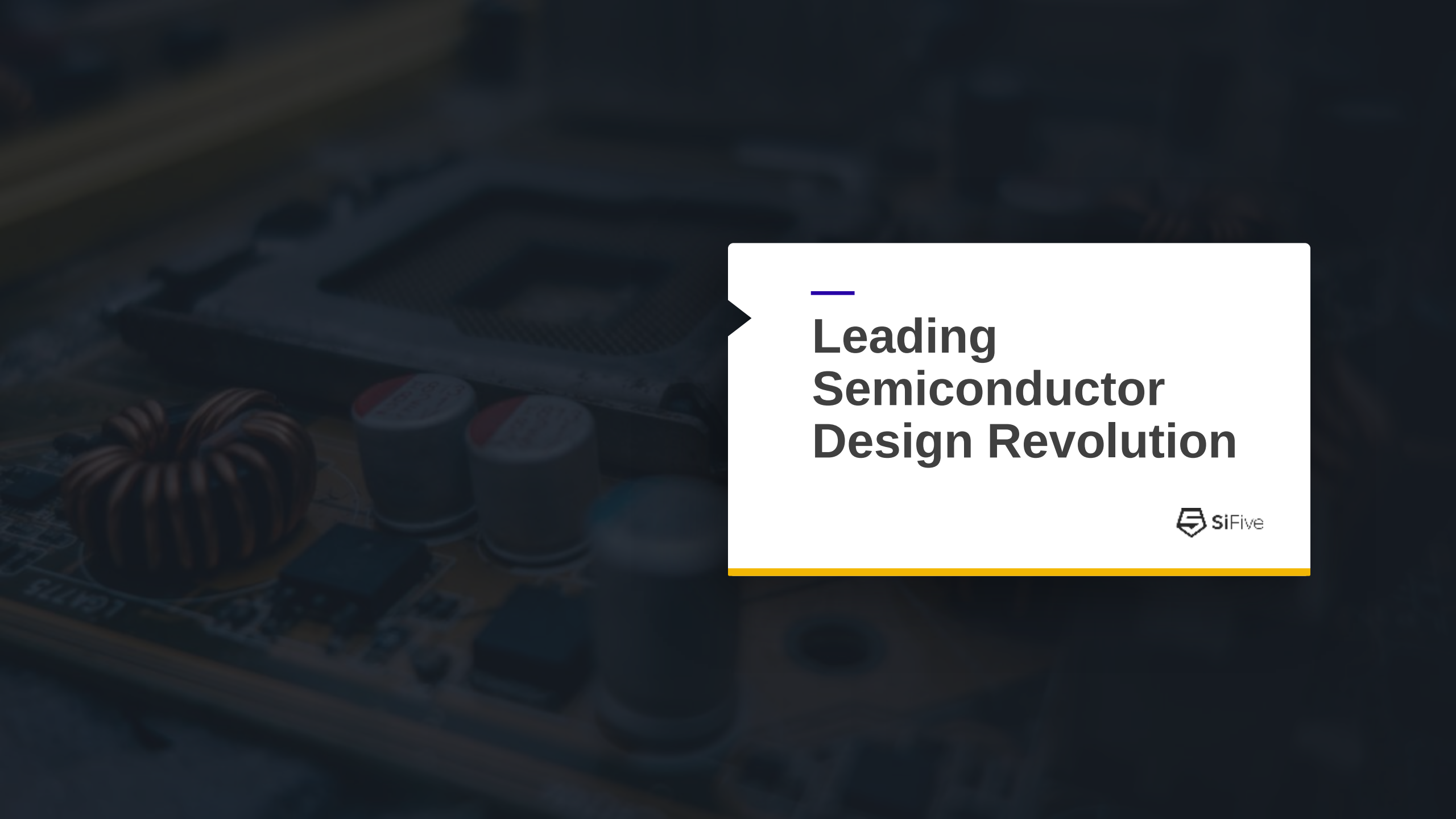
SiFive

Krste Asanovic

Co-Founder and Chief Architect



Leading Semiconductor Design Revolution

SiFive

SiFive - Global Presence and Reach

World Class Expertise

- Inventors of RISC-V
- Chip Design in the Cloud
- RTL, PD, Silicon
- Design Platforms

SiFive Worldwide Presence

- 15 Offices
- 400+ Employees
- 300+ Tapeouts

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We have assembled a World Class Team

Naveed Sherwani
President & CEO

Sunil Shenoy
SVP / GM IP BU

Shafy Eltoukhy
SVP / GM CSoC BU

Keith Witek
SVP Biz Dev & GC

Jay Vyas
CFO

Jack Kang
VP Sales

Yunsup Lee
CTO

Krste Asanovic
Chief Architect

Andrew Waterman
Chief Engineer

Jeff Mulhausen
Chief Evangelist

Thomas Xu
CEO, SaiFan China

Brandon Cho
CEO, SemiFive Korea

250 Years of Combined Experience in Semiconductors with 1,000s of Tape-Outs Founded by All 3 of the RISC-V Inventors

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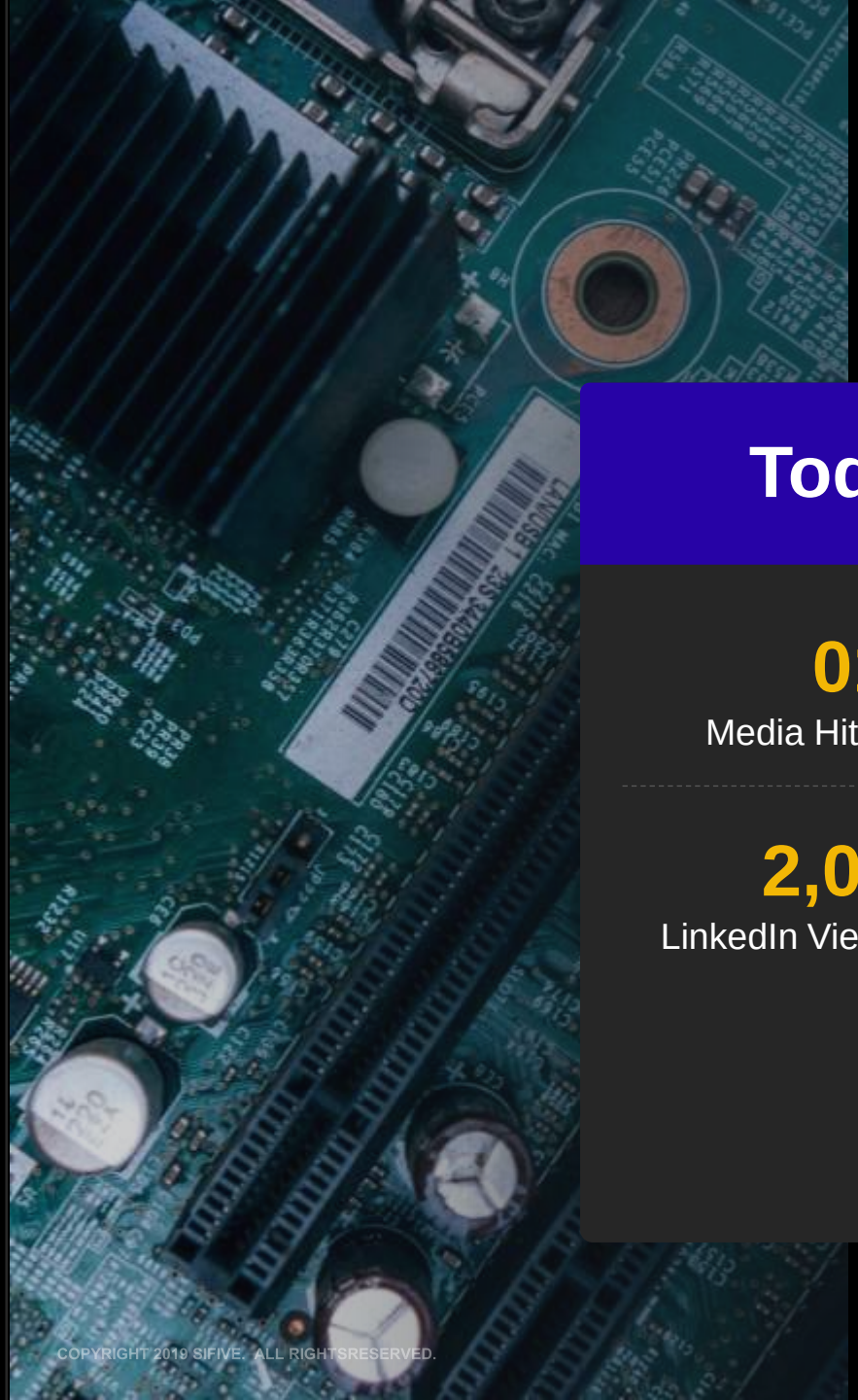

SiFive Momentum Unprecedented in the Semiconductor Industry

Today	This Week	This Year
01 Media Hit Per Day	**01** Press Release Per Week	**75** Cities
2,000 LinkedIn Views Per Day	**02** Global Events Per Week	**350** Talks
	200 Event Registrations	**6,000,000** Video Views

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GSA 2018 Award: SiFive Recognized as Most Respected Private Semiconductor Company

SiFive
Recognized as a Leader

- “More power-efficient than ARM’s competing processor designs”
- “A tenth of the price in a fifth of the time”
- “RISC-V on the Verge of Broad Adoption"
- “RISC-V Climbs Software Mountain”
- “Is the data center next?
- “SiFive Sees Big Year for RISC-V”
- “Anyone with a web interface will be able to design chips and solve problems”

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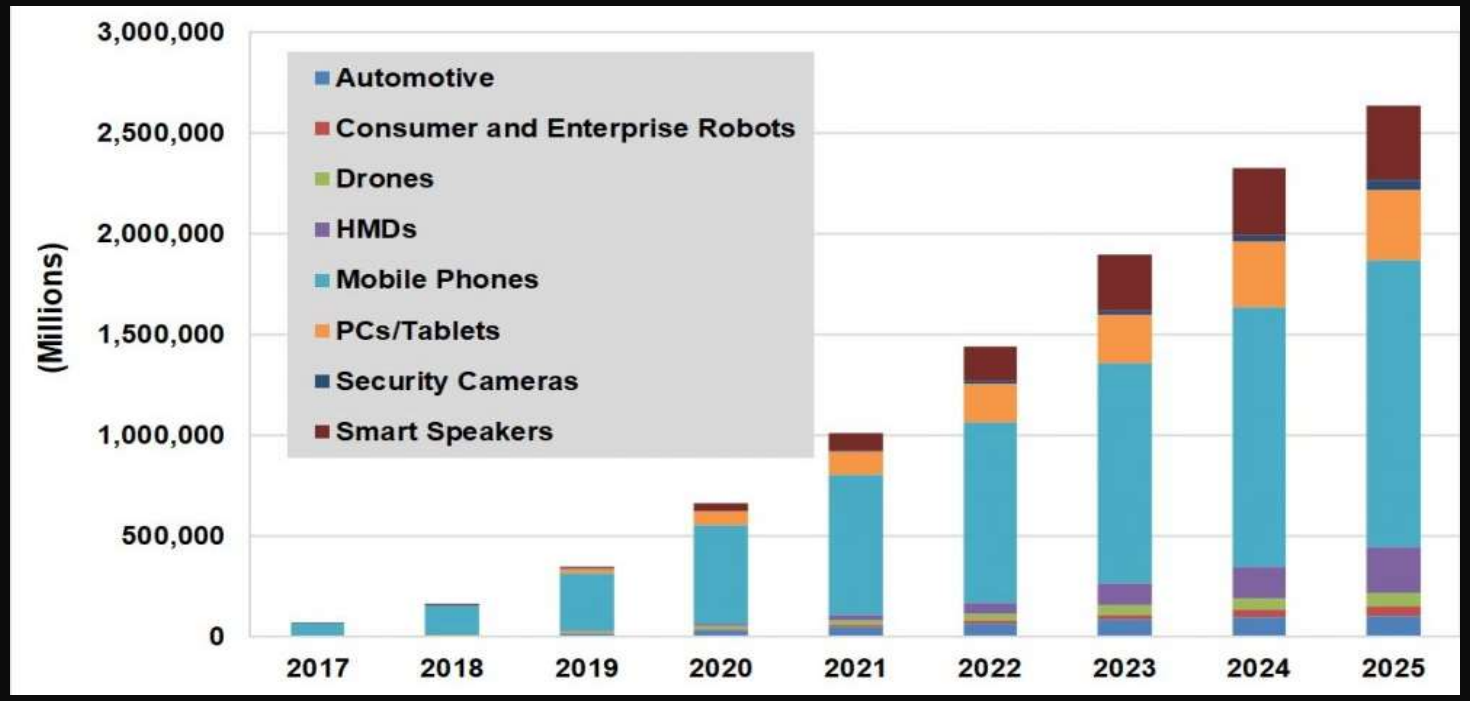
AI Edge Device Shipments – 3 Trillion by 2025

AI Edge Device Shipments by Category, 2017-2025



Source: Tractica

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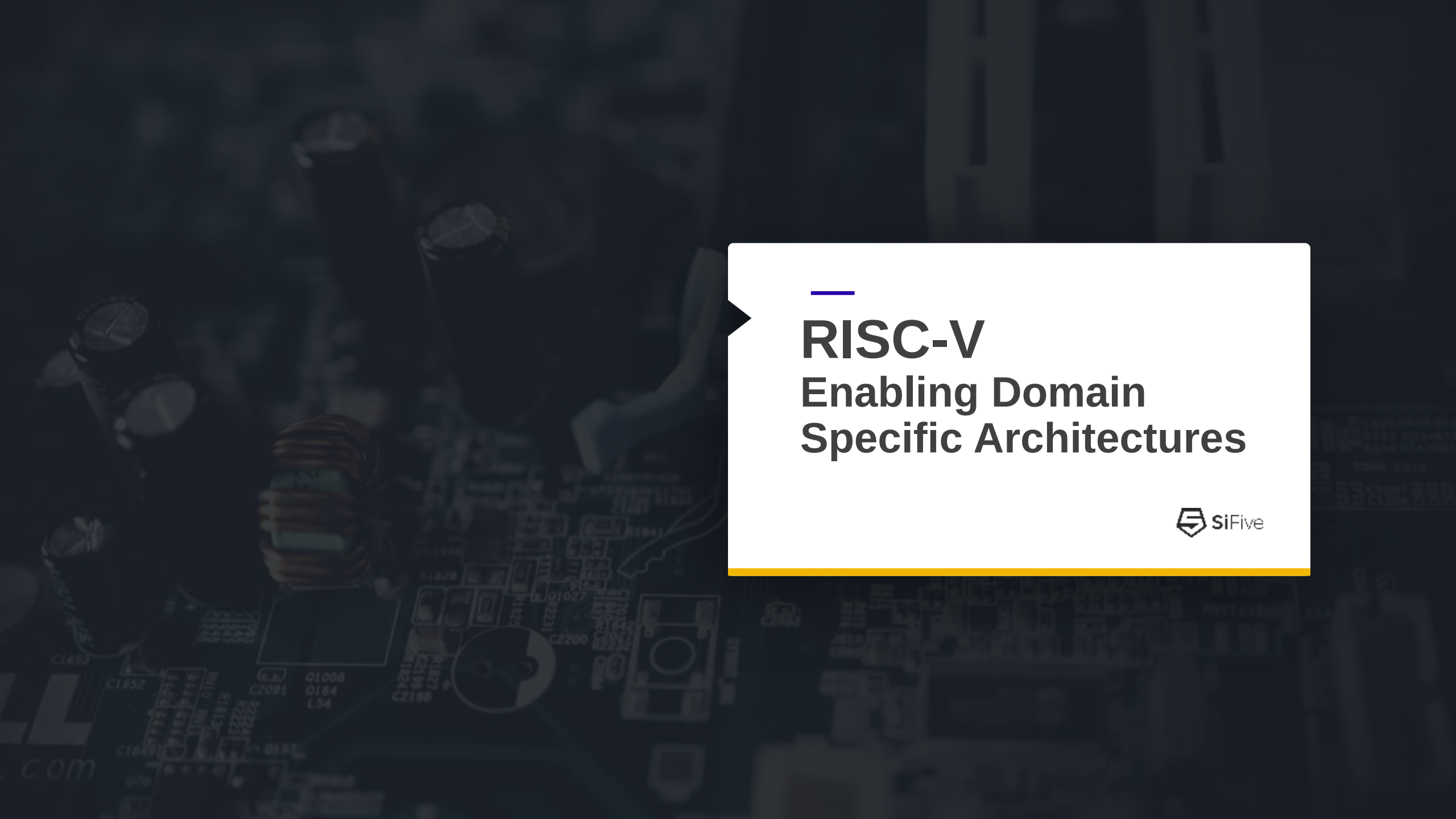

RISC-V
Enabling Domain Specific Architectures

SiFive

The RISC-V Promise

Simple, modern, modular ISA	Scales from microcontrollers to supercomputers
	Easily Extensible
Open Architecture	Freedom to choose
	Software ecosystem fostered by many
	Allowing differentiation, specialization, optimization

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SiFive RISC-V Core IP Product Series

E Cores | S Cores

Industry leading 32-bit and 64-bit Embedded Cores

7 Series High Performance Embedded	Storage Networking Automotive	S76 S76-MC E76 E76-MC
3/5 Series Small, Efficient, Performance	Industrial Modems Storage	S51 S54 E31 E34
2 Series SiFive's Most Efficient Series	Microcontrollers IoT Wearables	E21 E24 E20 S21

U Cores

High performance 64-bit Application Cores

7 Series Optimized High-Performance	SBC Networking Consumer	U74 U74-MC
5 Series Multi-Core RISC-V Linux	Low Cost Linux Industrial Gateways	U54-MC U54

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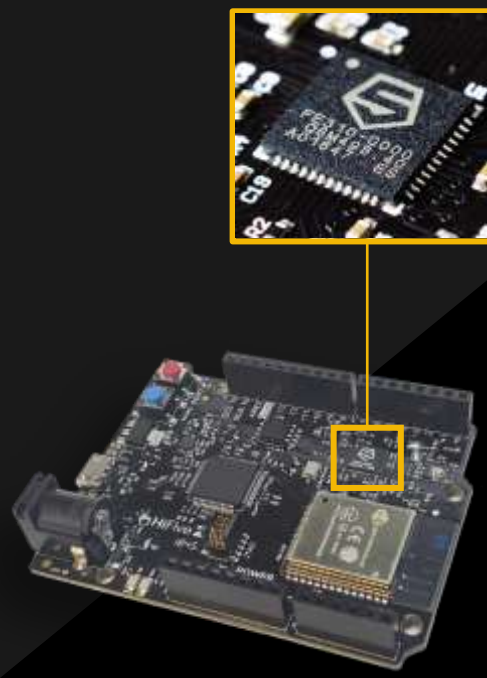
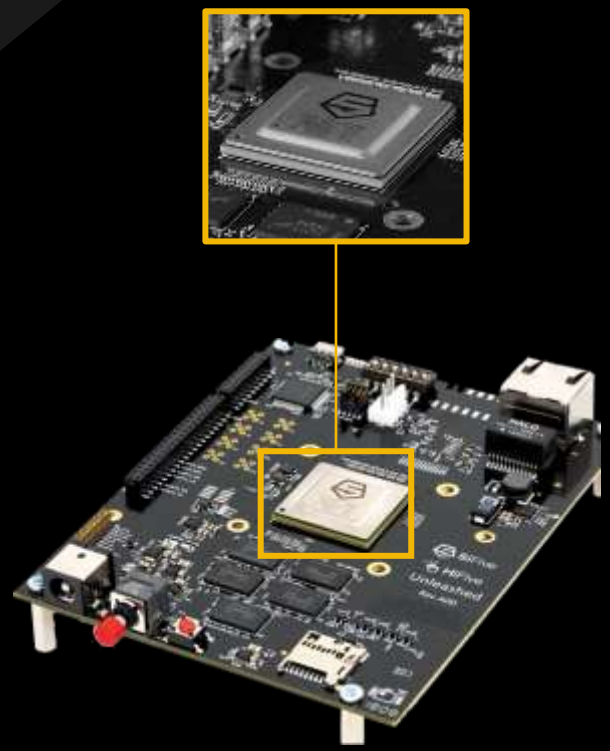
RISC-V Development Happens on HiFive Development Boards

HiFive1 RevB
FE310 (E31) Dev Kit



HiFive Unleashed + Expansion Board
World's First RISC-V Linux Dev Kit



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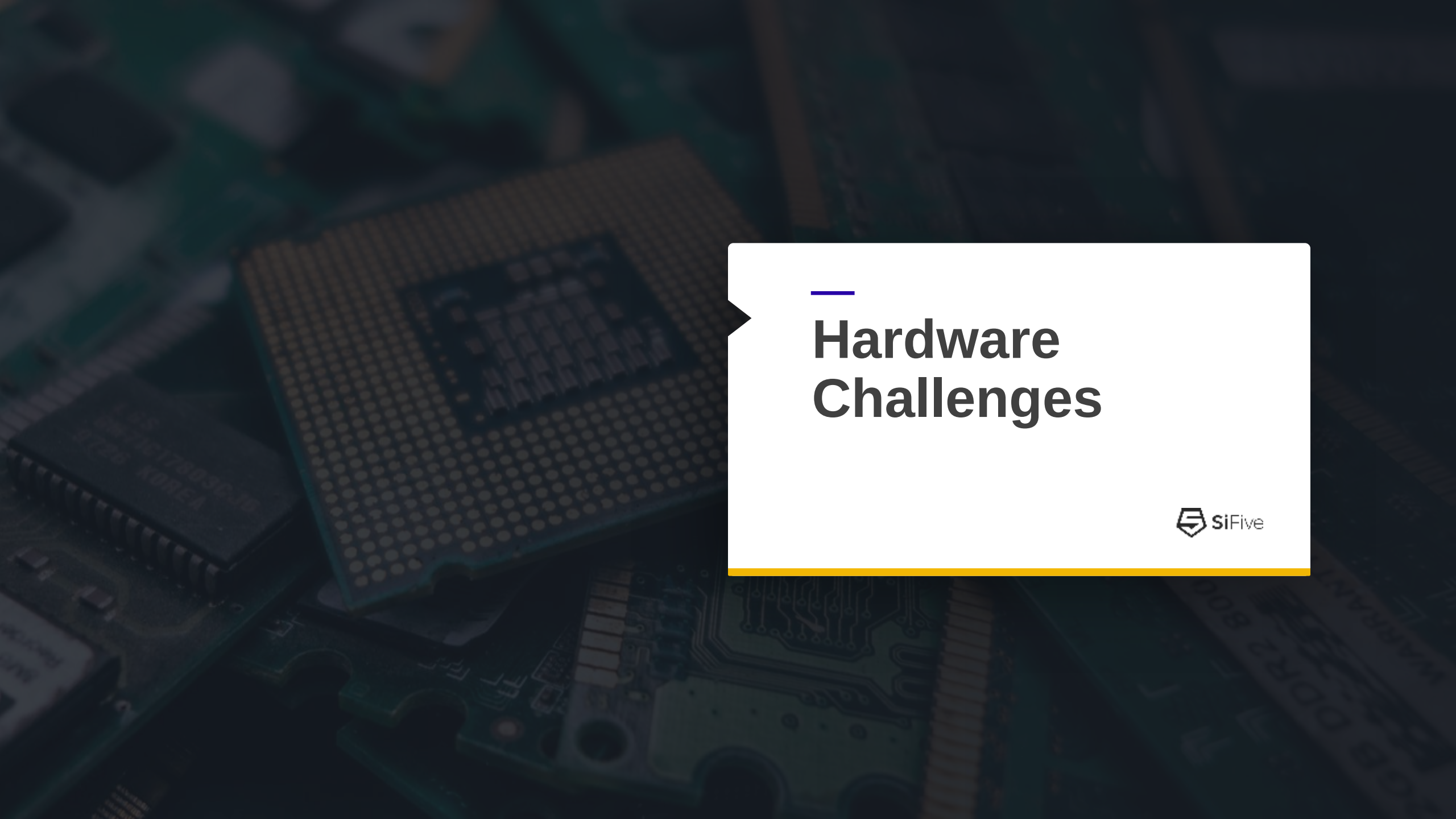


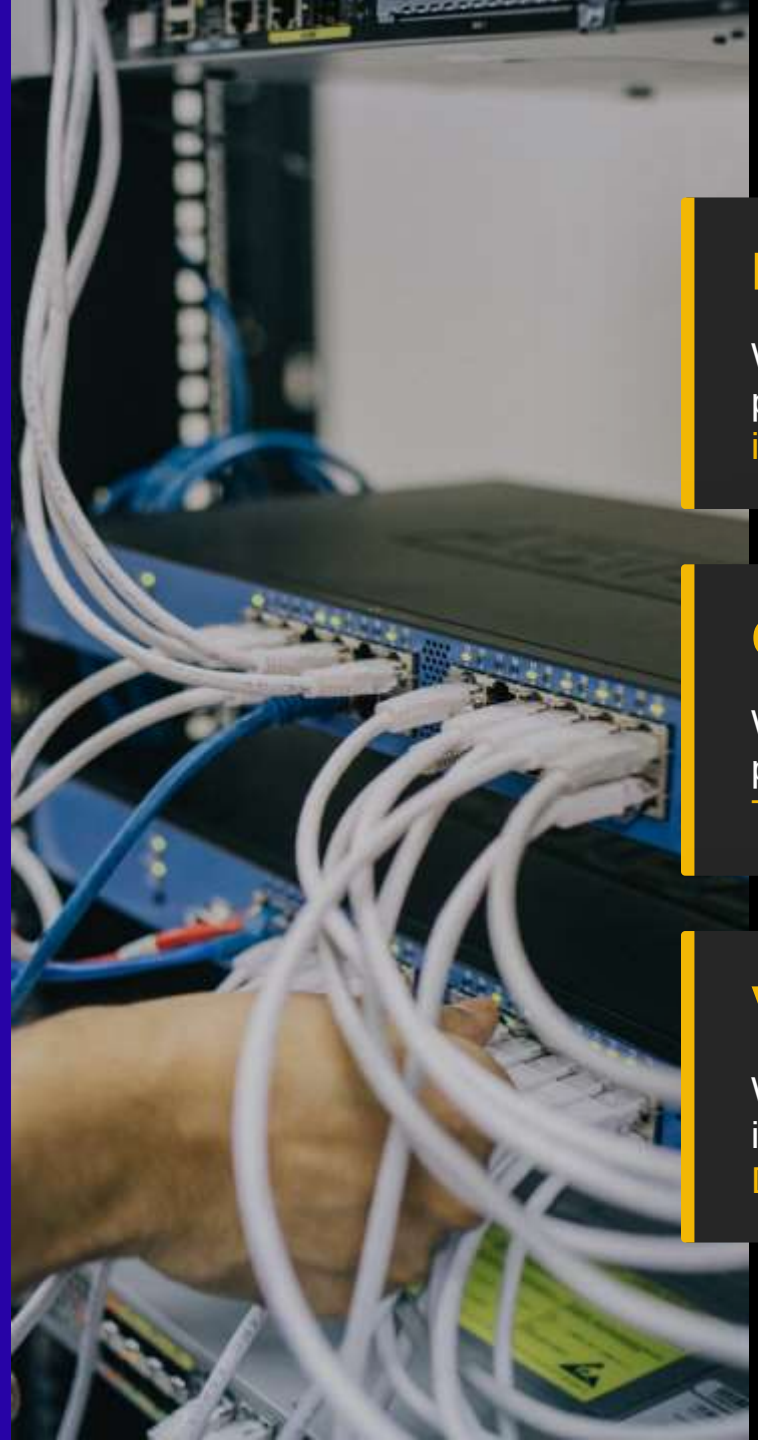
Hardware Challenges

SiFive

The Silicon Business is Ripe for Disruption!

Moore's Law is stalling, and customization is the only path forward for improved performance

And yet, the hardware innovation cycle is too slow, too expensive, and require too many experts under the same roof



RISC-V

We are leading the charge on enabling a new era of processor innovation with a free and open instruction set architecture

Custom Silicon

We are simplifying the custom silicon design process by encapsulating the complexities in Templates

Verticalization

We are empowering Software and Systems innovators with easy access to Templates via Designers on the cloud

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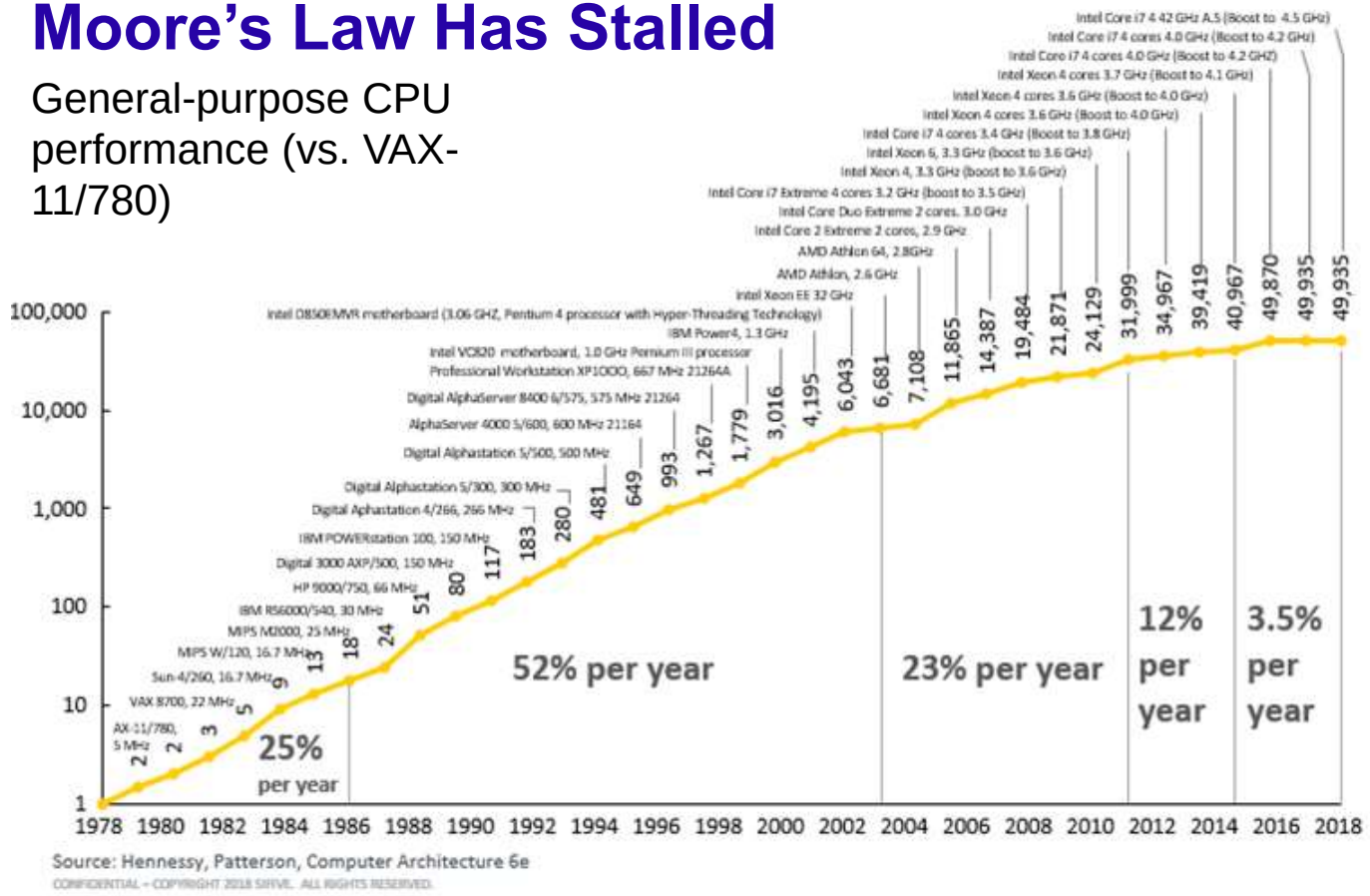
Why RISC-V, Customization and Verticalization?

Moore's Law Has Stalled

General-purpose CPU performance (vs. VAX-11/780)



Source: Hennessy, Patterson, Computer Architecture 6e

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Time for a Paradigm Shift

01 Customization is the only way to get performance

02 One-Chip-Fits-All no longer applies

03 Innovation is desperately needed to meet the needs of new applications running on billions of devices

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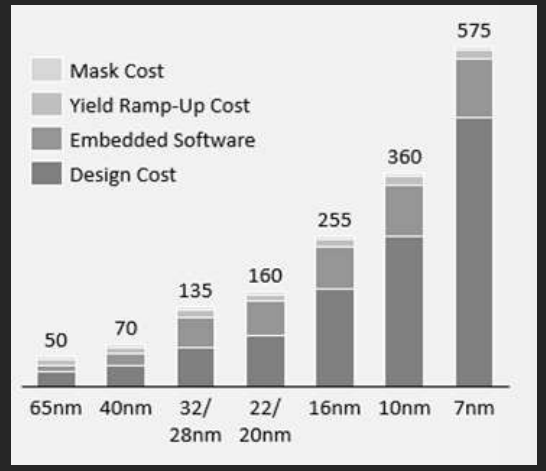
In hardware, Minimum Viable Products (MVPs) face 3 Significant Problems

Cost

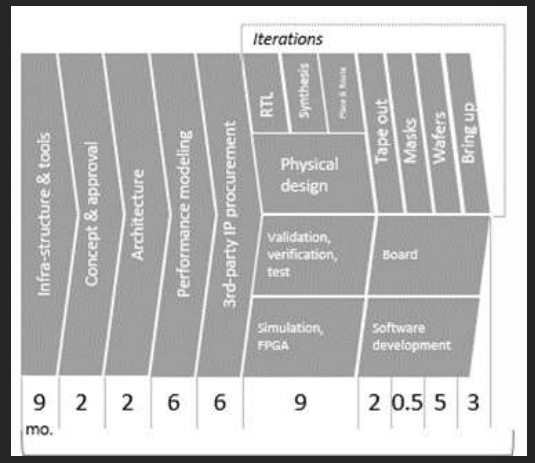
Chip Development Too Costly



$500M+ for 7nm

Time

Development Cycle Too Long



2 – 4 years

Expertise

Too Many Experts Needed

14+ Disciplines

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The SiFive Solution

SiFive

Why Do These Problems Not Exist in Software?

In software, Minimum Viable Products (MVPs) can be built very rapidly, by a small team, at low cost

Because the majority of stack exists!

Instagram

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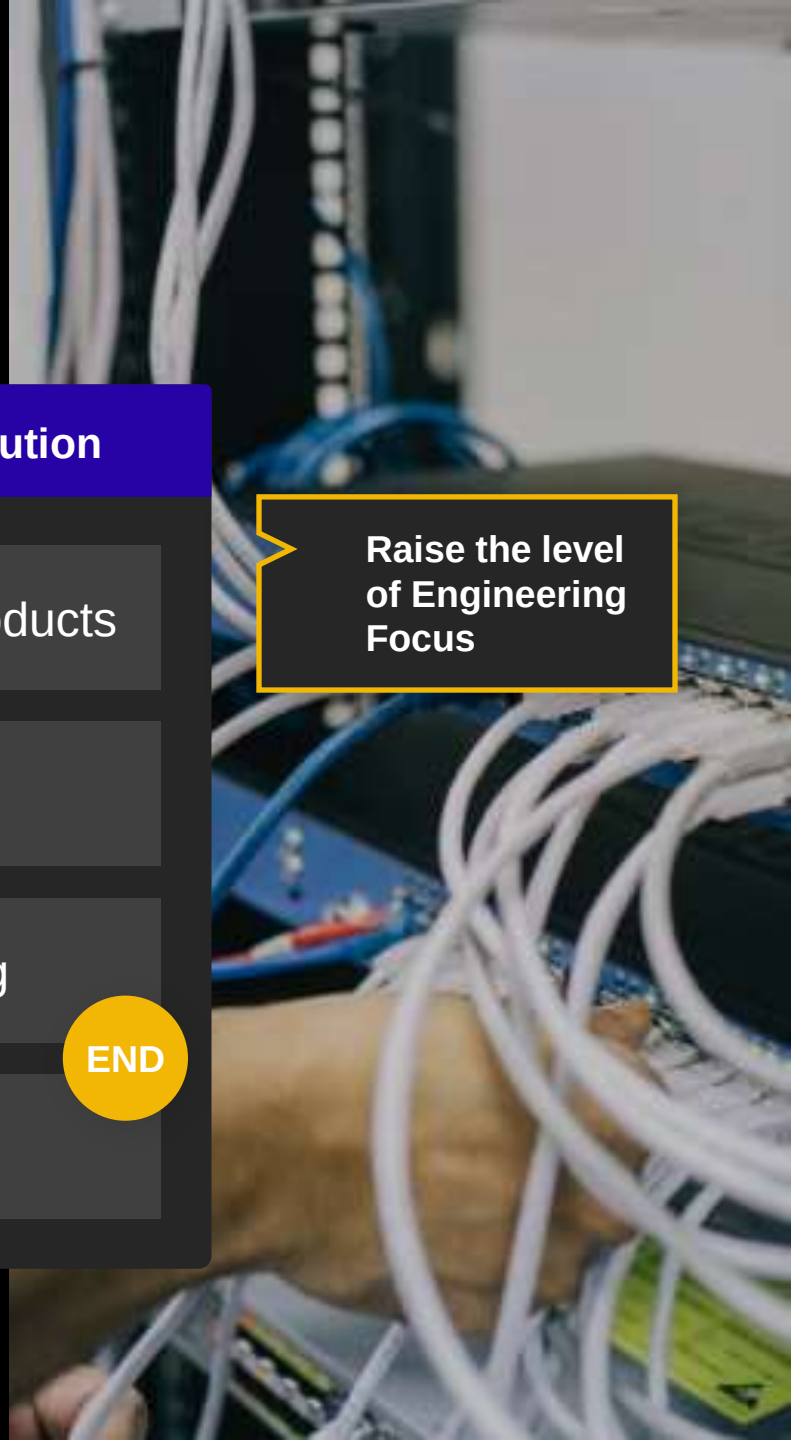
Learn from the success of Software

Software Industry	Semiconductor Industry	Semi Revolution
Apps		System Products
Java		Chisel
Assembly	Verilog	Verilog
Binary	GDSII	GDSII

END

END

END



Raise the level of Engineering Focus

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Software stack

- Customer IP (Application)
- API Framework
- Libraries
- Hardware Abstraction Layer
- OS Kernel
- Hardware

"Hardware stack"

- Customer IP (Chip)
- Core/Block/Chip Configurators/Generators
- Chip Templates
- Chisel
- EDA Tools
- Hardware

Innovators focus on high-level work

"Hardware Stack" Disrupting the Silicon Business at Software Speed

Source: Google Developers

Foundry / OSAT

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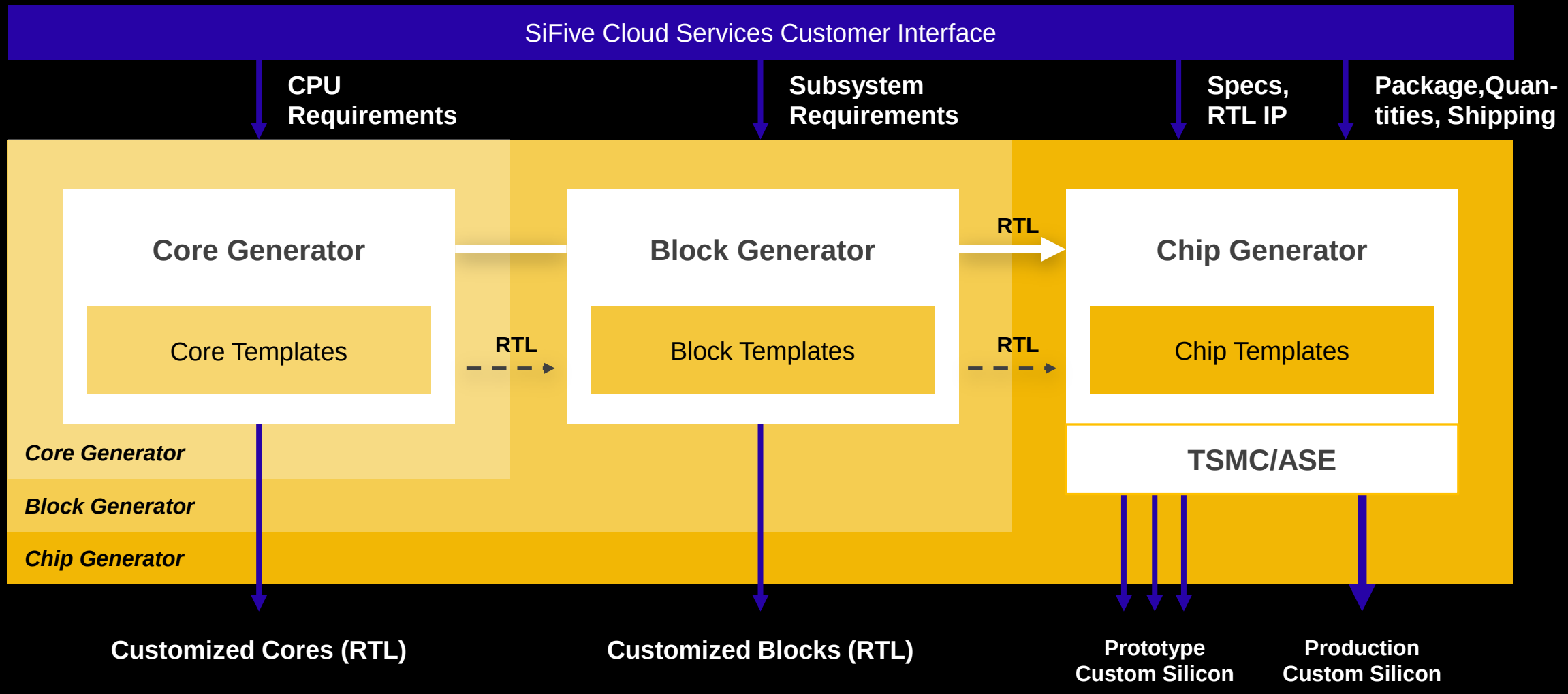
We Provide Customizable Cores, Blocks and Chips on the Cloud



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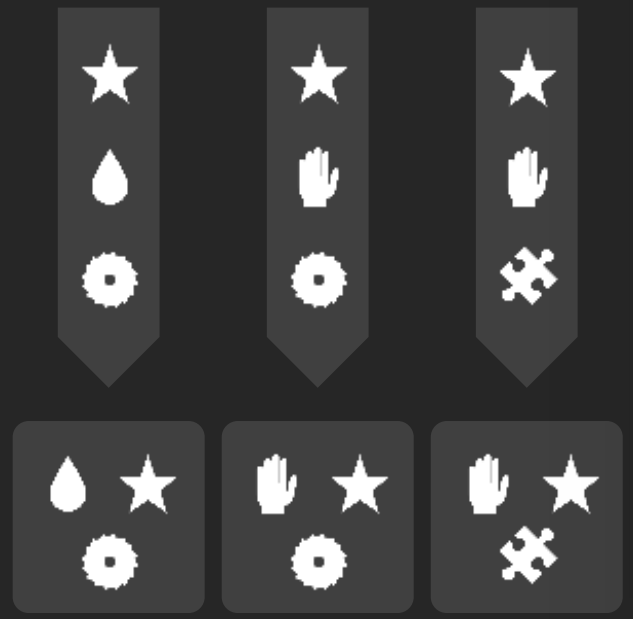
We Simplify the Design Process by Encapsulating Complexities in Templates

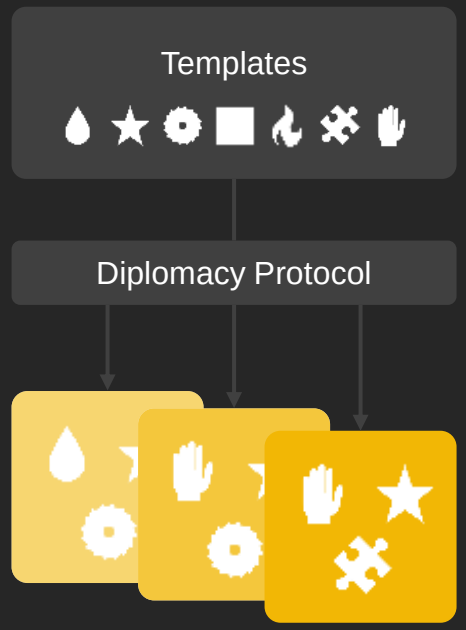
Traditional Approach:
Iterative Addition

Build individual building blocks and add them to a chip



The SiFive Approach:
Iterative Subtraction to Reconfigure Cores, Blocks, and Chips

Subtract from Templates (Predesigned Supersets)



Template Methodology used across Cores, Blocks and Chips

Core Templates	Block Templates	Chip Templates
E2 Series	Core Complex	AI accelerator
E3 Series	TileLink Interconnect	SmartNIC
U7 Series	HBM Controller	IoT Hub
E20/E21	U54 Core Complex	Custom AI Chip
E31	Tilelink over Ethernet	Optimized NIC
U74	Custom HBM	Voice IoT Hub

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DesignShare Enables Rapid Scaling of IP Pool Needed to Build Templates

IP Easily Integratable

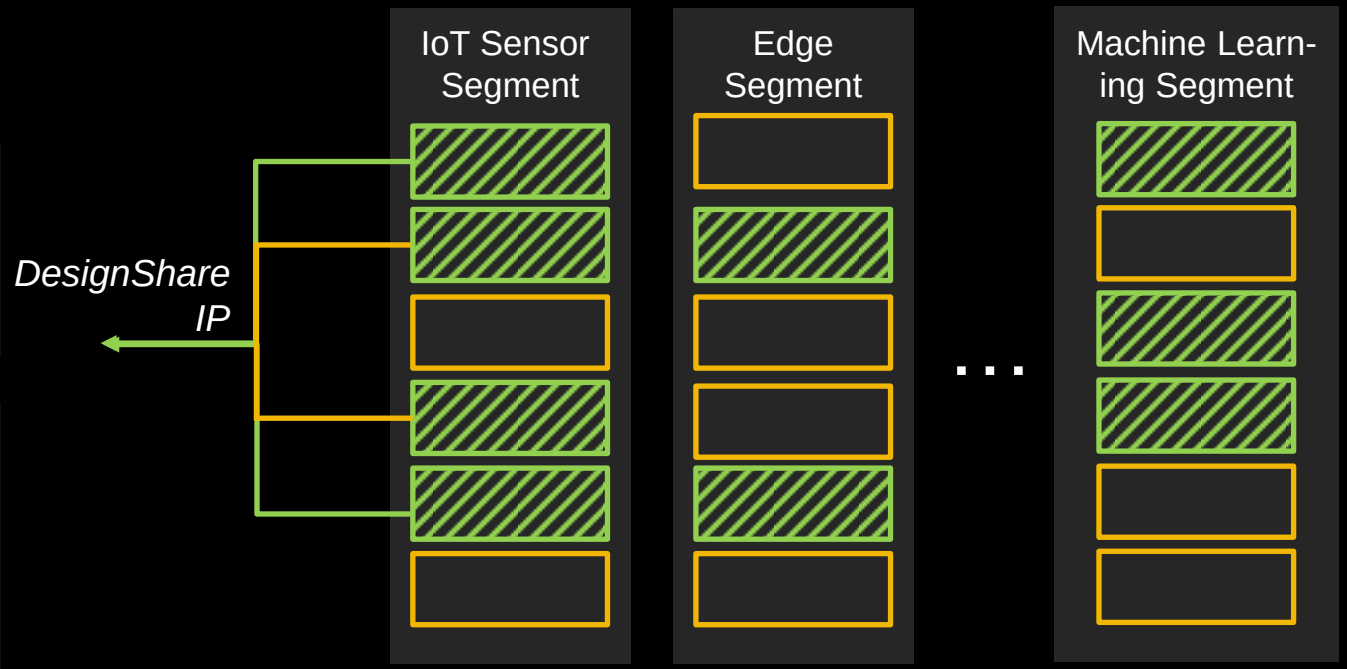
DesignShare Partners provide their IP for SiFive Freedom Platform at zero cost

Benefit to DesignShare Partners

- Increase number of design starts
- IP Protection
- SiFive collects NRE/Royalties in production

Benefits to Customers

- Reduces expertise needed
- Single contract/NDA



Rambus · Think Silicon · Analog Bits · DOVER · Corigine · chipus · ultraSoC · flexlogix · Brite · mobivel · ememory · Wasiela · SECURE RF · ASIC Design Services · OPENEDGES

DesignShare Partners
20+ in the Pipeline….

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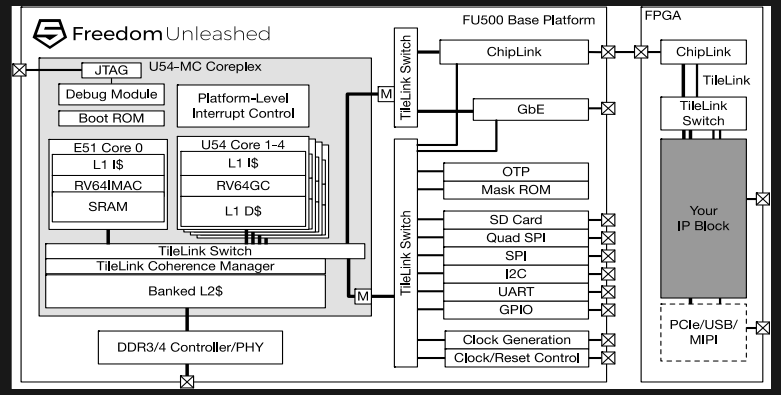
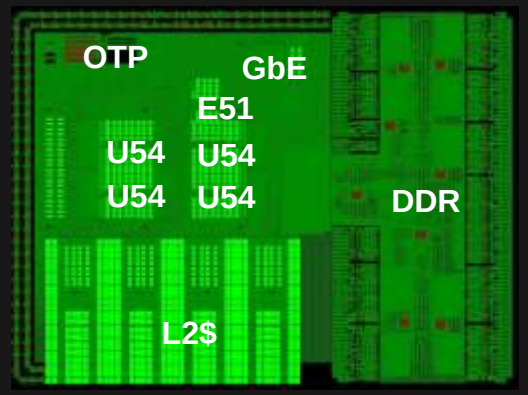
Our Approach Has Produced Many World's Firsts

World's First Cloud Tape-Out with Microsoft





1.5+ GHz U54-MC SiFive CPU
1x E51: 16KB L1I$, 8KB DTIM with ECC support
4x U54: 32KB L1I$, 32KB L1D$ with ECC support
ChipLink
Serialized Chip-to-Chip Coherent TileLink Interconnect
DDR3/4, GbE, Peripherals

World's First RISC-V SSD Controller

SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products."

– Jihyo Lee, FADU CEO

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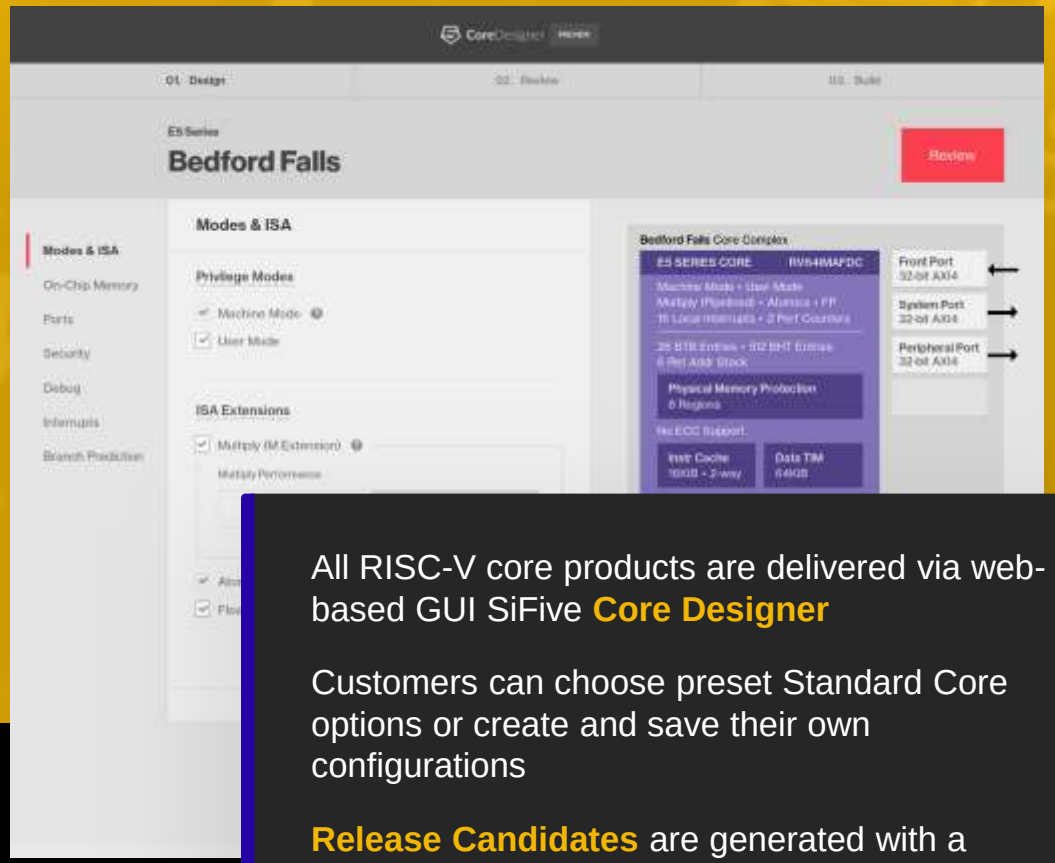
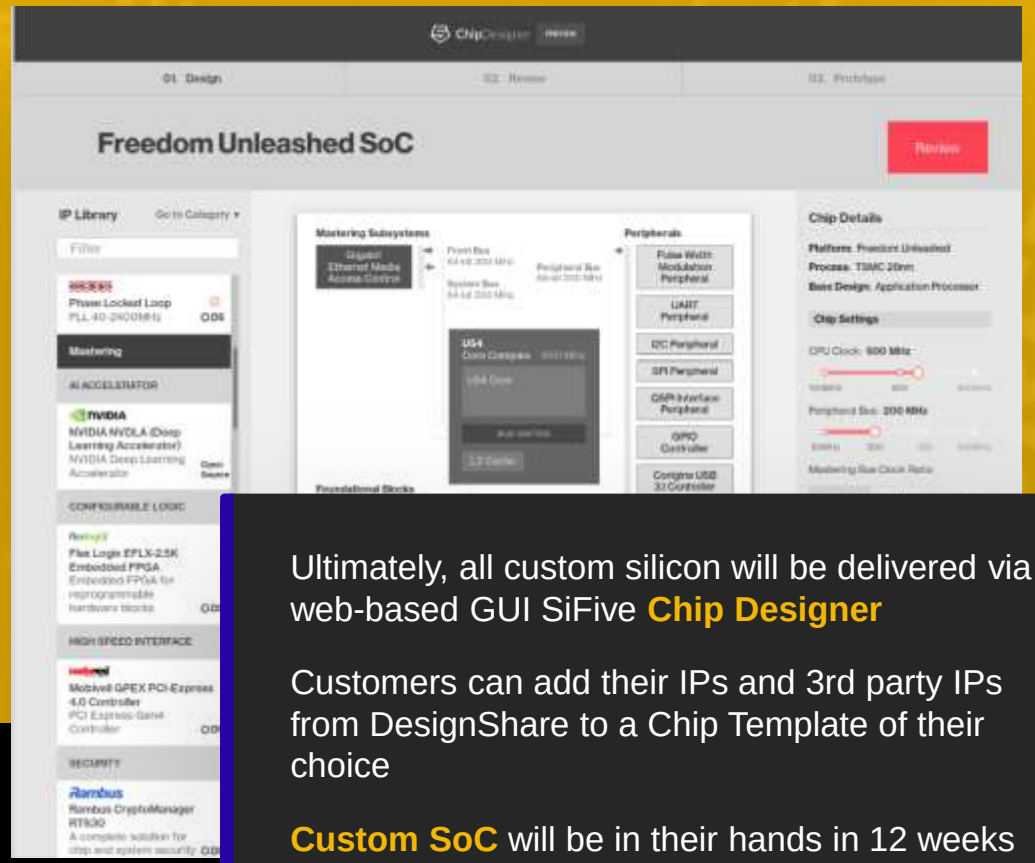
Core Designer & Chip Designer



All RISC-V core products are delivered via web-based GUI SiFive **Core Designer**

Customers can choose preset Standard Core options or create and save their own configurations

Release Candidates are generated with a single click and available in 24 hours after verification



Ultimately, all custom silicon will be delivered via web-based GUI SiFive **Chip Designer**

Customers can add their IPs and 3rd party IPs from DesignShare to a Chip Template of their choice

Custom SoC will be in their hands in 12 weeks with a single click

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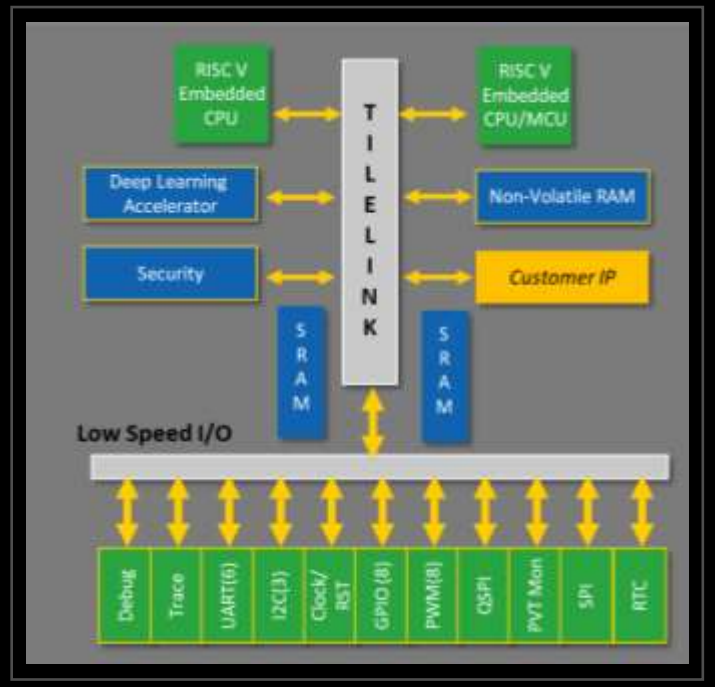
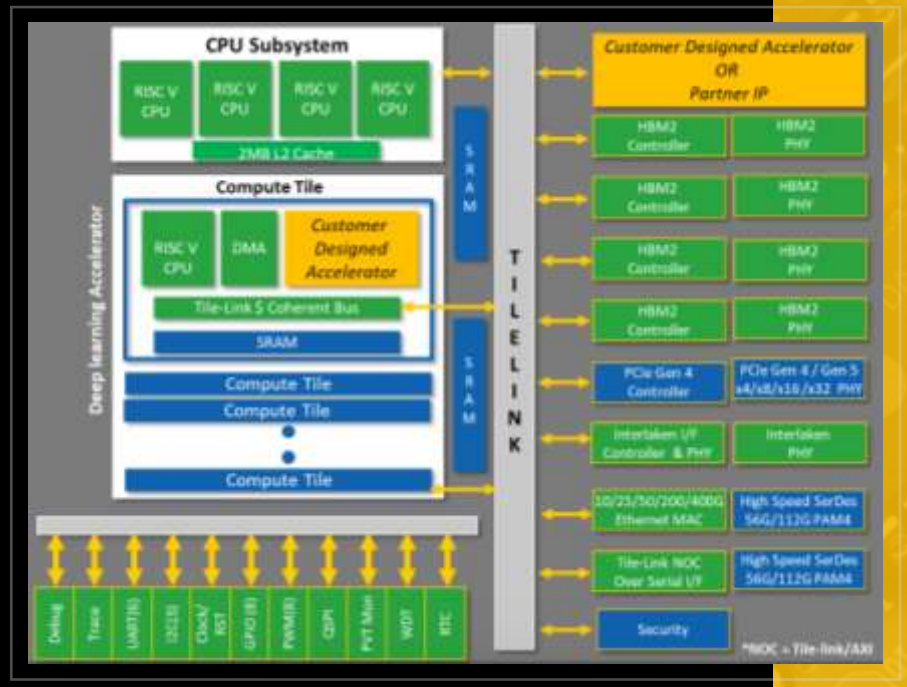
SiFive Freedom Platforms

28nm Freedom Aware



7nm Freedom Revolution



Ultra-low power solutions optimized for consumer and industrial IoT applications.

April 11, 2019

SiFive Tapes Out First in a Series of 7nm IP Enablement Platforms

—

Includes critical IP validation for HBM3E 3.2Gbps Interface, TCAM and more

Legend

- SiFive IP
- Customer IP
- Partner IP
- SiFive Custom SoC

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SiFive Leverages Cloud to Accelerate IP/Blocks/Chips to Market!

Customize IP

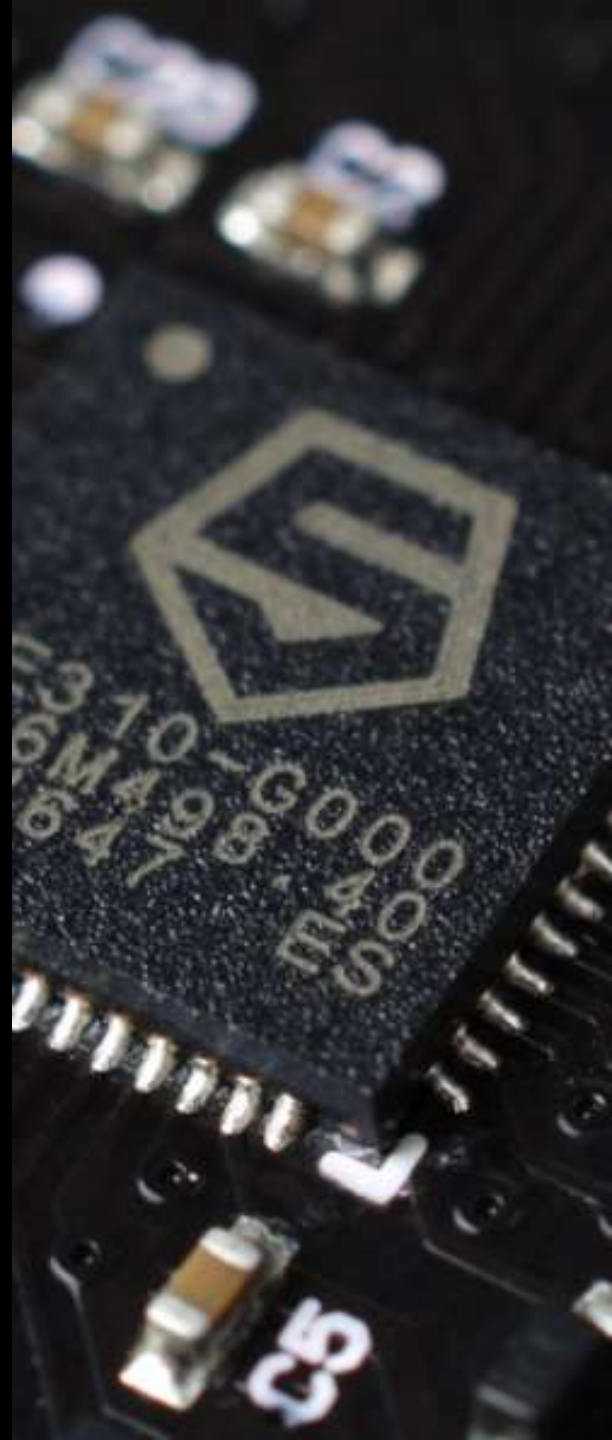
- All RISC-V core products are delivered via web-based GUI SiFive **Core Designer**

Customize Blocks

- Ultimately, all blocks will be delivered via web-based GUI SiFive **Block Designer**

Customize Chips

- Ultimately, all custom silicon will be delivered via web-based GUI **Chip Designer**



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Thank You!

SiFive

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